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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,571	07/18/2003	Tae-Jung Lee	2557-000160/US	2114

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,571	LEE ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 25-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 26-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledge is made of applicants' claim for foreign priority base on an application 2003-1815 filed in Korea on 01/11/203.

It is noted that Applicants have filled a certified copy of said application as required by U.S.C 119, which papers have been placed of record in the file.

Election/Restriction

2. Examiner confirms that Applicants elected to prosecute Claims 1-11, 26-30 and have withdrawn Claims 12-24 without prejudice.

Claim 25 has been amended to include limitations of claim 1, claim 25 is depended on withdrawn claim (non-elected claim 12), therefore, claim 25 is not considered and not examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 6, 9-10, 26-29 are rejected under 35 USC 102 (e) as being anticipated by Na et al., U.S. Patent No. 6,849,506 (DIV of Pat. No. 6,649,967 filed on Jun. 5, 2001).

Regarding claims 1, 26, 27, Na et al. discloses a cell structure of non-volatile memory device (See Figs. 1-5l and Cols. 1-10) using a nitride layer as a floating gate spacer comprising: a gate stack including a first portion 36 a of a floating gate formed over a semiconductor substrate, a control gate 38a formed over at least part of the first portion of the floating gate, and an exposed non-nitride spacer 42 (oxide/oxidation resist) adjacent to sidewalls of the first portion of the floating gate, a floating gate transistor including a second portion 33 of the floating gate formed over the semiconductor substrate having source/drain impurities implanted on both sides of the second portion of the floating gate, it is inherent that the impurities migrated to area of the substrate including the area under the second portion of the floating gate, therefore the second portion of floating gate is overlapped at least portion of source/drain region,

a nitride spacer formed on sidewall of the second portion 13 of the floating gate (Cols. 2-3).

Regarding claims 2-3, Na et al. discloses wherein the floating gate transistor further includes an insulating pattern including a nitride layer 37 between the control gate and first portion of the floating gate and a nitride spacer adjacent to sidewalls of the second portion of the floating gate.

Regarding claim 6, Na et al. discloses the first and second portion of floating (36a, 33) comprises polysilicon doped with impurity ions.

Regarding claim 9, Na et al. further discloses wherein the non-volatile memory device is at least one of an erasable programmable read only memory device and a flash memory device (Cols. 1-4).

Regarding claims 10, 28, Na et al. discloses the wherein at least one of the source/drain is operated to inject charges into the floating gate via hot carrier injection thereby programming a cell in the non-volatile memory (Col. 7).

Regarding claim 29, Na et al. discloses at least one of the source and drain is inject the charge via hot carrier injection. It is inherent that the control gate is to receive a first voltage and source/drain region and second portions of floating gate receive a second voltage.

6. Claims 4-5, 7-8, 11, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Na et al., U.S. Pat. No. 6,849,506.

Regarding claims 4, 11, 30 Na et al. discloses the first portion of the floating gate is operable to discharge the injected charges to the at lest one of an implanted source/drain and also discloses the non-nitride spacers including oxide film 41 and oxidation resist insulation film 40 but fails to disclose one of the spacer is polysilicon. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use polysilicon material as a spacer because the diffusion constant of polysilicon is high and resistivity is low, and because polysilicon has grain boundaries are rich in incomplete bonds, free carriers can be trapped at its grain boundaries to discharge the injected charges, the carries become deplete, therefore the programmable cell is erasable when ultraviolet rays applied to the polysilicon.

Regarding claims 7-8, Na et al. discloses an insulating pattern between the second portion of the floating gate and substrate is insulating material and the controle gate is polysilicon but fails to teach the insulating material including at least one of ONO or NO layer and the control gate also include silicide. It is well known in the art that ONO or NO material is used to form insulating material in non-volatile memory cell and the control gate also include silicide layer to minimize resistance of the gate.

Regarding claim 5, Na et al. fails to disclose a nitride spacer adjacent to sidewalls of the control gate. However, it would have been obvious to one having ordinary skill in the art to use nitride or non-nitride to form a spacer adjacent to sidewalls of the control gate because it would not change the functions/manners/characteristics of the control gate in the non-volatile memory device.

7. If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

8. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le

Examiner

Art Unit 2818